Efficient CRC-BCH Unified Encoder for Global Positioning System

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Abstract

GPS uses ECCs to see if an error occurs when the data sent from the satellite reaches the user. Each message structure uses ECCs such as Hamming Code, CRC, BCH Code, and LDPC Code. If the satellite contains all of the encoders, it has a negative impact to the area and power consumption. Therefore, in this paper, we propose a CRC-BCH unified encoder for GPS, which is efficient in terms of space and power consumption. Since both the CRC and BCH encoders use shift registers, the design was made using this part. To replace the existing encoder, the CRC-BCH encoder must have the same output. To validate this, we used individual CRC and BCH encoders and confirmed that the generated output was identical to the output of the proposed encoder. The proposed CRC-BCH unified encoder was synthesized at an operating frequency of 400 MHz using the CMOS 28nm process. The synthesis results showed that it used 16.67% less area and consumed 19.68% less power than the existing encoder. Therefore, the proposed CRC-BCH unified encoder offers advantages in terms of satellite weight and energy efficiency.

Keywords: GPS, ECC, CRC, BCH, Encoder

1. Introduction

The Global Navigation Satellite System (GNSS) is a service that provides information on the position, velocity, and time (PVT) of receivers using signals transmitted by satellites in Earth's orbit. Currently, various countries provide GNSS, including Russia's GLONASS, China's BeiDou, and Europe's Galileo. Among them, the most notable GNSS is the Global Positioning System (GPS). GPS is a GNSS provided by the United States and has been available to the public since the 1980s. It is still widely used by many people today.

When GPS satellites transmit signals in orbit, the signals may be exposed to various environments. This environment provides the user with the possibility of containing errors different from the data transmitted by the satellite when received [1]. Therefore, GPS uses an Error Correction Code (ECC) that can check whether there is an error in the received signal. The ECCs used in GPS are Hamming Code, Cyclic Redundancy Check (CRC), Bose-Chaudhuri-Hocquenghem (BCH) Code, and Low-Density Parity Check (LDPC) Code. They depend on what message structure GPS uses, including Hamming Code in Legacy Navigation (LNAV) message structure, CRC in Civil Navigation (CNAV) message structure, and CRC, BCH Code, and LDPC in CNAV-2 message structure [2-3]. Therefore, there should be a circuit inside the GPS satellite that can encode these four ECCs. However, having many circuits can increase weight and power consumption of the satellite. If the shared part of each encoder is considered and integrated into one encoder, area and power consumption can be reduced. Therefore, this paper proposes a power and area-efficient CRC-BCH unified encoder that combines the two encoder circuits into one. The encoders of the two ECCs were integrated using shift registers. In addition, comparisons are made in terms of area and power used compared to when existing CRC and BCH encoders are used separately.

2. Background

CRC is an ECC using the properties of cyclic codes [4]. There are two main advantages of the CRC. One is that encoders can be designed relatively easily using shift registers using the nature of cyclical codes. The second is that it is robust not only to random errors but also to burst errors, which occur continuously.

Mathematically, CRC can be generated using the generator polynomial $g(X)$. Regardless of the message structure, the CRC used in GPS employs $g(X) = X^{24} + X^{23} + X^{18} + X^{17} + X^{14} + X^{11} + X^{10} + X^7 + X^6 + X^5 + X^4 + X^3 + X + 1$. Using these generator polynomials, 24 parity bits can be generated regardless of the

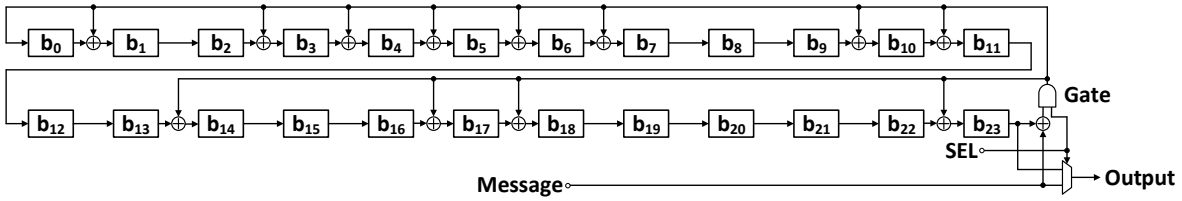

Figure 1. Conventional CRC-24Q encoder.

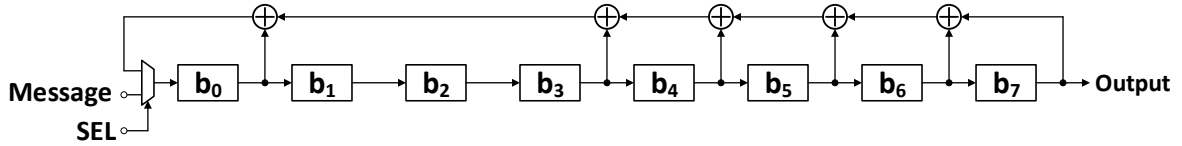

Figure 2. Conventional BCH (51, 8) encoder.

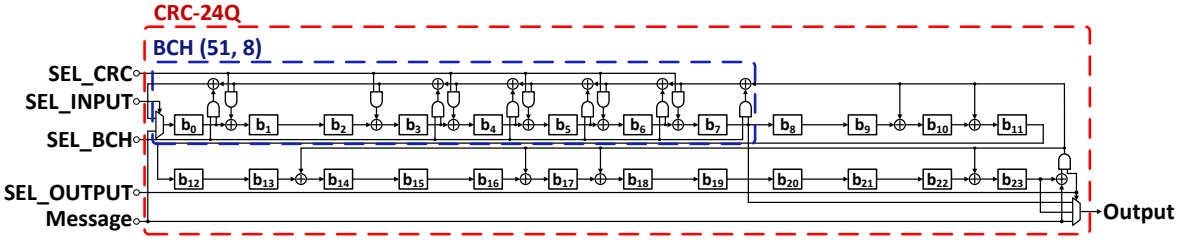

Figure 3. Proposed CRC-BCH unified encoder.

length of the input message. This specific generator polynomial-based CRC is referred to as CRC-24Q [2]. The process of CRC encoding can be represented as Equation (1).

$$X^{n-k}\mathbf{u}(X)+\mathbf{b}(X)=\mathbf{a}(X)\mathbf{g}(X). \quad (1)$$

$X^{n-k}\mathbf{u}(X)$ is the result of multiplying the message $\mathbf{u}(X)$ by X^{n-k}, which can also be understood as shifting the message by $n-k$ bits. Here, k means the number of parity bits added, and n means the number of bits of the symbol encoded by adding the parity bit. Dividing $X^{n-k}\mathbf{u}(X)$ by the generator polynomial $g(X)$ yields the remainder, the polynomial $\mathbf{b}(X)$. This remainder is then added to $X^{n-k}\mathbf{u}(X)$ to complete the encoding. The added polynomial $\mathbf{b}(X)$ becomes the parity bits.

The process of obtaining the remainder through polynomial division can be implemented using a shift register. The encoding circuit for CRC-24Q is shown in figure 1. Based on a total of 24 shift registers initialized to a value of 0, each tap's position is determined by the coefficients of $g(X)$. When the message to be encoded enters from the input message, it performs an XOR operation with the output of b_{23}, and this result becomes the feedback value. While the input message is being fed into the register, the output is directly from the input message. After the entire input message is registered, the gate output is set to zero, ensuring the feedback remains zero, and the remaining values in the register are output bit by bit. These remaining values in the register correspond to the coefficients of the remainder in the mathematical formulation and serve as the parity bits.

BCH code is also a type of cyclic code. However, unlike the CRC, it is constituted of polynomials based on the extended Galois field $\mathrm{GF}(2^m)$ [4]. Due to its cyclic property, the BCH code can also be encoded using a shift register. The BCH code used in CNAV-2 is BCH (51, 8), meaning that an 8-bit message is encoded into 51 encoded symbols.

To generate these symbols, the generator polynomial $g(X)=X^8+X^7+X^6+X^5+X^4+X+1$ is used [3]. Figure 2 illustrates the BCH (51, 8) encoder as described in the GPS Interface Control Document (ICD). As with CRC, the position of the tap is determined by the generator polynomial. The encoding process is as follows: starting with a shift register initialized to a value of 0, an 8-bit message is fed from the most significant bit (MSB). After the entire 8-bit input is registered, 51 shifts are executed, resulting in 51 outputs from the b_7 register. The initial 8 bits of the output remain identical to the original values. Thereafter, 43 bits calculated by the shift register are output. These 43 bits that came out at the end become parity bits.

3. Proposed CRC-BCH Unified Encoder

Figure 3 illustrates the proposed CRC-BCH unified encoder. Using the fact that both the traditional CRC-24Q encoder and BCH (51, 8) encoder use shift registers for encoding, the design

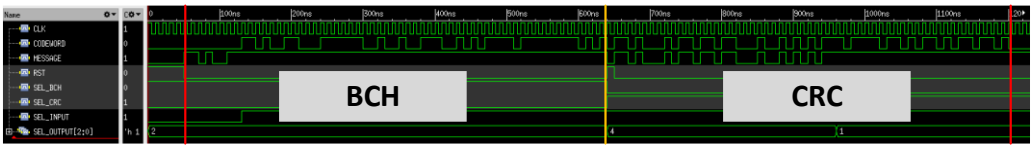

Figure 4. Simulation result.

was optimized to share registers. Since the CRC-24Q encoder employs 24 registers, it was designed to encompass the BCH encoder. However, given the differences in the generator polynomial and directions of tap between BCH and CRC, AND gates were utilized to control and set the appropriate tap directions for each condition. To relay the BCH output, the output section of the b_7 register was connected to the CRC output section. with a multiplexer introduced to select which value is outputted. The choice between encoding CRC or BCH is determined using SEL_CRC and SEL_BCH.

Table 1. Synthesis results of the conventional encoder and the proposed encoder.

	Conventional (CRC+BCH)	Proposed
Critical Path Delay [ns]	1.15	1.33
Equivalent Gate Count	120.74 (88.92+31.82)	100.619
Power [μW]	72.64 (55.71+16.93)	58.345

4. Experimental Result

To replace the existing encoder with the proposed CRC-BCH unified encoder, the output generated by each encoder must match the output from the CRC-BCH encoder. Therefore, we first implemented conventional CRC-24Q and BCH (51, 8) encoders to check the output. Based on the respective encoders of CRC-24Q and BCH (51, 8) implemented, it was confirmed whether the output of the proposed CRC-BCH unified encoder was the same. As a result of simulation to check whether the circuit is operating normally, it was confirmed that the correct output was produced according to each set mode as shown in Figure 4. Subsequently, CMOS 28nm was used in the synthesis process, and the operating frequency was set to 400 MHz. In order to compare the area of the conventional and proposed structures, an equivalent gate count obtained by dividing the total area by the size of the two-input NAND gate was used, and the power consumption of the two structures was confirmed using the synthesis results. Based on the results presented in Table 1, the proposed structure reduced the area by 16.67% and the total power consumption by 19.68%, confirming that the proposed CRC-BCH unified provides advantages in terms of area and power consumption over the existing design.

5. Conclusion

In this paper, we proposed a CRC-BCH unified encoder for GPS to reduce power consumption and area. Taking advantage of the fact that both CRC and BCH encoders use shift registers, we integrated the BCH encoder into the CRC encoder structure, which requires more registers. Additionally, we added a circuit to select between CRC and BCH encoding based on the desired encoding method. To compare the performance with the existing encoders, synthesis was carried out using the CMOS 28nm process. Experimental results confirmed that the proposed structure offers advantages in terms of area and power consumption compared to the traditional design. Therefore, we believe that satellites using the proposed CRC-BCH unified encoder would have superior weight efficiency compared to current satellites.

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